Precision Instrumentation Amplifier

AD524

FEATURES

Low noise: 0.3 µV p-p at 0.1 Hz to 10 Hz
Low nonlinearity: 0.003% (G = 1)
High CMRR: 120 dB (G = 1000)
Low offset voltage: 50 µV
Low offset voltage drift: 0.5 µV/°C
Gain bandwidth product: 25 MHz
Pin programmable gains of 1, 10, 100, 1000
Input protection, power-on/power-off
No external components required
Internally compensated
MIL-STD-883B and chips available
16-lead ceramic DIP and SOIC packages and 20-terminal leadless chip carrier available
Available in tape and reel in accordance with EIA-481A standard
Standard military drawing also available

FUNCTIONAL BLOCK DIAGRAM

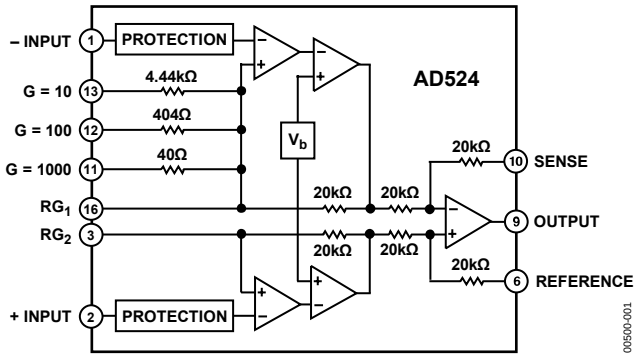


Figure 1.

GENERAL DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common-mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25 µV/°C, input offset voltage drift of less than 0.5 µV/°C, CMR above 90 dB at unity gain (120 dB at G = 1000), and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications, the AD524 also has a 25 kHz bandwidth (G = 1000). To make it suitable for high speed data acquisition systems, the AD524 has an output slew rate of 5 V/µs and settles in 15 µs to 0.01% for gains of 1 to 100.

As a complete amplifier, the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1000. For other gain settings between 1 and 1000, only a single resistor is required. The AD524 input is fully protected for both power-on and power-off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical A grade, the low drift B grade, and lower drift, higher linearity C grade are specified from −25°C to +85°C. The S grade guarantees performance to specification over the extended temperature range −55°C to +125°C. The AD524 is available in a 16-lead ceramic DIP, 16-lead SBDIP, 16-lead SOIC wide packages, and 20-terminal leadless chip carrier.

PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift, and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100, and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power-on and power-off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25 MHz, full power response of 75 kHz and a settling time of 15 µs to 0.01% of a 20 V step (G = 100).

Rev. F

SPECIFICATIONS

@ V_S = ±15 V, R_L = 2 kΩ and T_A = +25°C, unless otherwise noted.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at the final electrical test. Results from those tests are used to calculate outgoing quality levels.

Table 1.

	AD524A			AD524B			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
GAIN							
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000		
Gain Error[1]							
G = 1			**±0.05**			**±0.03**	%
G = 10			**±0.25**			**±0.15**	%
G = 100			**±0.5**			**±0.35**	%
G = 1000			**±2.0**			**±1.0**	%
Nonlinearity							
G = 1			±0.01			±0.005	%
G = 10, G = 100			±0.01			±0.005	%
G = 1000			±0.01			±0.01	%
Gain vs. Temperature							
G = 1			5			5	ppm/°C
G = 10			15			10	ppm/°C
G = 100			35			25	ppm/°C
G = 1000			100			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)							
Input Offset Voltage			**250**			**100**	µV
vs. Temperature			2			**0.75**	µV/°C
Output Offset Voltage			5			**3**	mV
vs. Temperature			100			**50**	µV
Offset Referred to the Input vs. Supply							
G = 1	**70**			**75**			dB
G = 10	**85**			**95**			dB
G = 100	**95**			**105**			dB
G = 1000	**100**			**110**			dB
INPUT CURRENT							
Input Bias Current			**±50**			**±25**	nA
vs. Temperature		±100			±100		pA/°C
Input Offset Current			**±35**			**±15**	nA
vs. Temperature		±100			±100		pA/°C

Parameter	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	Unit
INPUT							
Input Impedance							
Differential Resistance		10^9			10^9		Ω
Differential Capacitance		10			10		pF
Common-Mode Resistance		10^9			10^9		Ω
Common-Mode Capacitance		10			10		pF
Input Voltage Range							
Maximum Differential Input Linear (V_{DL})[2]	±10			±10			V
Maximum Common-Mode Linear (V_{CM})[2]	$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			V
Common-Mode Rejection DC to 60 Hz with 1 kΩ Source Imbalance							V
G = 1	**70**			**75**			dB
G = 10	**90**			**95**			dB
G = 100	**100**			**105**			dB
G = 1000	**110**			**115**			dB
OUTPUT RATING							
V_{OUT}, R_L = 2 kΩ		±10			±10		V
DYNAMIC RESPONSE							
Small Signal – 3 dB							
G = 1		1			1		MHz
G = 10		400			400		kHz
G = 100		150			150		kHz
G = 1000		25			25		kHz
Slew Rate		5.0			5.0		V/µs
Settling Time to 0.01%, 20 V Step							
G = 1 to 100		15			15		µs
G = 1000		75			75		µs
NOISE							
Voltage Noise, 1 kHz							
RTI		7			7		nV/√Hz
RTO		90			90		nV√Hz
RTI, 0.1 Hz to 10 Hz							
G = 1		15			15		µV p-p
G = 10		2			2		µV p-p
G = 100, 1000		0.3			0.3		µV p-p
Current Noise							
0.1 Hz to 10 Hz		60			60		pA p-p
SENSE INPUT							
R_{IN}		20			20		kΩ ± 20%
I_{IN}		15			15		µA
Voltage Range	±10			±10			V
Gain to Output		1			1		%
REFERENCE INPUT							
R_{IN}		40			40		kΩ ± 20%
I_{IN}		15			15		µA
Voltage Range	±10			±10			V
Gain to Output		1			1		%

Parameter	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	Unit
TEMPERATURE RANGE							
Specified Performance	–25		+85	–25		+85	°C
Storage	–65		+150	–65		+150	°C
POWER SUPPLY							
Power Supply Range	**±6**	±15	**±18**	**±6**	±15	**±18**	V
Quiescent Current		3.5	**5.0**		3.5	**5.0**	mA

[1] Does not include effects of external resistor, R_G.
[2] V_{OL} is the maximum differential input voltage at G = 1 for specified nonlinearity.
V_{DL} at the maximum = 10 V/G.
V_D = actual differential input voltage.
Example: G = 10, V_D = 0.50.
V_{CM} = 12 V – (10/2 × 0.50 V) = 9.5 V.

@ V_S = ±15 V, R_L = 2 kΩ and T_A = +25°C, unless otherwise noted.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at the final electrical test. Results from those tests are used to calculate outgoing quality levels.

Table 2.

Parameter	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Unit
GAIN							
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000		
Gain Error[1]							
G = 1			**±0.02**			**±0.05**	%
G = 10			**±0.1**			**±0.25**	%
G = 100			**±0.25**			**±0.5**	%
G = 1000			**±0.5**			**±2.0**	%
Nonlinearity							
G = 1			±0.003			±0.01	%
G = 10, G = 100			±0.003			±0.01	%
G = 1000			±0.01			±0.01	%
Gain vs. Temperature							
G = 1			5			5	ppm/°C
G = 10			10			10	ppm/°C
G = 100			25			25	ppm/°C
G = 1000			50			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)							
Input Offset Voltage			**50**			**100**	µV
vs. Temperature			**0.5**			**2.0**	µV/°C
Output Offset Voltage			**2.0**			**3.0**	mV
vs. Temperature			**25**			**50**	µV
Offset Referred to the Input vs. Supply							
G = 1	**80**			**75**			dB
G = 10	**100**			**95**			dB
G = 100	**110**			**105**			dB
G = 1000	**115**			**110**			dB

Parameter	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Unit
INPUT CURRENT							
Input Bias Current			**±15**			**±50**	nA
vs. Temperature		±100			±100		pA/°C
Input Offset Current			**±10**			**±35**	nA
vs. Temperature		±100			±100		pA/°C
INPUT							
Input Impedance							
Differential Resistance		10^9			10^9		Ω
Differential Capacitance		10			10		pF
Common-Mode Resistance		10^9			10^9		Ω
Common-Mode Capacitance		10			10		pF
Input Voltage Range							
Maximum Differential Input Linear (V_{DL})[2]	±10			±10			V
Maximum Common-Mode Linear (V_{CM})[2]	$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			V
Common-Mode Rejection DC to 60 Hz with 1 kΩ Source Imbalance							V
G = 1	**80**			**70**			dB
G = 10	**100**			**90**			dB
G = 100	**110**			**100**			dB
G = 1000	**120**			**110**			dB
OUTPUT RATING							
V_{OUT}, R_L = 2 kΩ		±10			±10		V
DYNAMIC RESPONSE							
Small Signal – 3 dB							
G = 1		1			1		MHz
G = 10		400			400		kHz
G = 100		150			150		kHz
G = 1000		25			25		kHz
Slew Rate		5.0			5.0		V/µs
Settling Time to 0.01%, 20 V Step							
G = 1 to 100		15			15		µs
G = 1000		75			75		µs
NOISE							
Voltage Noise, 1 kHz							
RTI		7			7		nV/√Hz
RTO		90			90		nV√Hz
RTI, 0.1 Hz to 10 Hz							
G = 1		15			15		µV p-p
G = 10		2			2		µV p-p
G = 100, 1000		0.3			0.3		µV p-p
Current Noise							
0.1 Hz to 10 Hz		60			60		pA p-p
SENSE INPUT							
R_{IN}		20			20		kΩ ± 20%
I_{IN}		15			15		µA
Voltage Range	±10			±10			V
Gain to Output		1			1		%

Parameter	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Unit
REFERENCE INPUT							
R_{IN}		40			40		kΩ ± 20%
I_{IN}		15			15		µA
Voltage Range	10			10			V
Gain to Output		1			1		%
TEMPERATURE RANGE							
Specified Performance	–25		+85	–55		+85	°C
Storage	–65		+150	–65		+150	°C
POWER SUPPLY							
Power Supply Range	**±6**	±15	**±18**	**±6**	±15	**±18**	V
Quiescent Current		3.5	**5.0**		3.5	**5.0**	mA

[1] Does not include effects of external resistor R_G.
[2] V_{OL} is the maximum differential input voltage at G = 1 for specified nonlinearity.
V_{OL} at the maximum = 10 V/G.
V_D = actual differential input voltage.
Example: G = 10, V_D = 0.50.
V_{CM} = 12 V – (10/2 × 0.50 V) = 9.5 V.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation	450 mW
Input Voltage[1]	
(Either Input Simultaneously) $\|V_{IN}\| + \|V_S\|$	<36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
(R)	−65°C to +125°C
(D, E)	−65°C to +150°C
Operating Temperature Range	
AD524A/AD524B/AD524C	−25°C to +85°C
AD524S	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	+300°C

[1] Maximum input voltage specification refers to maximum voltage to which either input terminal may be raised with or without device power applied. For example, with ±18 volt supplies maximum, V_{IN} is ±18 V; with zero supply voltage maximum, V_{IN} is ±36 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

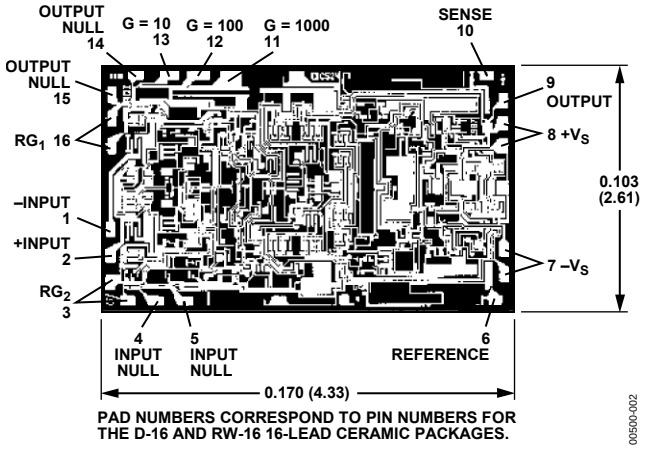


Figure 2. Metallization Photograph
Contact factory for latest dimensions;
Dimensions shown in inches and (mm)

CONNECTION DIAGRAMS

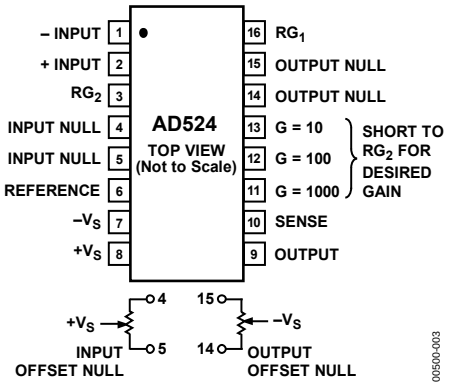


Figure 3. Ceramic (D) and
SOIC (RW-16 and D-16) Packages

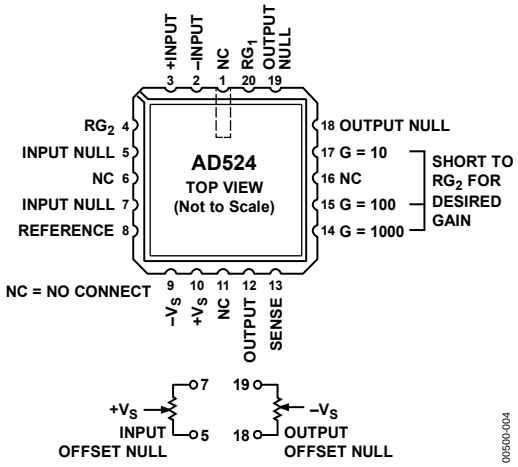


Figure 4. Leadless Chip Carrier (E)

ESD CAUTION

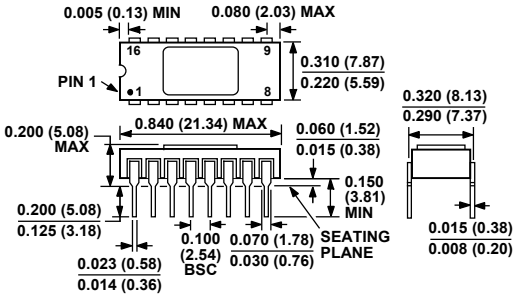
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 5. Error Budget Analysis

Error Source	AD524C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.25%	±0.25% = 2500 ppm	2500 ppm	2500 ppm	–
Gain Instability	25 ppm	(25 ppm/°C)(60°C) = 1500 ppm	–	1500 ppm	–
Gain Nonlinearity	±0.003%	±0.003% = 30 ppm	–	–	30 ppm
Input Offset Voltage	±50 µV, RTI	±50 µV/20 mV = ±2500 ppm	2500 ppm	2500 ppm	–
Input Offset Voltage Drift	±0.5 µV/°C –	(±0.5 µV/°C)(60°C) = 30 µV 30 µV/20 mV = 1500 ppm	–	1500 ppm	–
Output Offset Voltage[1]	±2.0 mV	±2.0 mV/20 mV = 1000 ppm	1000 ppm	1000 ppm	–
Output Offset Voltage Drift[1]	±25 µV/°C	(±25 µV/°C)(60°C)= 1500 µV 1500 µV/20 mV = 750 ppm	–	750 ppm	–
Bias Current-Source Imbalance Error	±15 nA	(±15 nA)(100 Ω) = 1.5 µV 1.5 µV/20 mV = 75 ppm	75 ppm	75 ppm	–
Bias Current-Source Imbalance Drift	±100 pA/°C	(±100 pA/°C)(100 Ω)(60°C) = 0.6 µV 0.6 µV/20 mV = 30 ppm	–	30 ppm	–
Offset Current-Source Imbalance Error	±10 nA	(±10 nA)(100 Ω) = 1 µV 1 µV/20 mV = 50 ppm	50 ppm	50 ppm	–
Offset Current-Source Imbalance Drift	±100 pA/°C	(100 pA/°C)(100 Ω)(60°C) = 0.6 µV 0.6 µV/20 mV = 30 ppm	–	30 ppm	–
Offset Current-Source Resistance-Error	±10 nA	(10 nA)(175 Ω) = 3.5 µV 3.5 µV/20 mV = 87.5 ppm	87.5 ppm	87.5 ppm	–
Offset Current-Source Resistance-Drift	±100 pA/°C	(100 pA/°C)(175 Ω)(60°C) = 1 µV 1 µV/20 mV = 50 ppm	–	50 ppm	–
Common Mode Rejection 5 V DC	115 dB	115 dB = 1.8 ppm × 5 V = 8.8 µV 8.8 µV/20 mV = 444 ppm	444 ppm	444 ppm	–
Noise, RTI (0.1 Hz to 10 Hz)	0.3 µV p-p	0.3 µV p-p/20 mV = 15 ppm	–	–	15 ppm
		Total Error	6656.5 ppm	10516.5 ppm	45 ppm

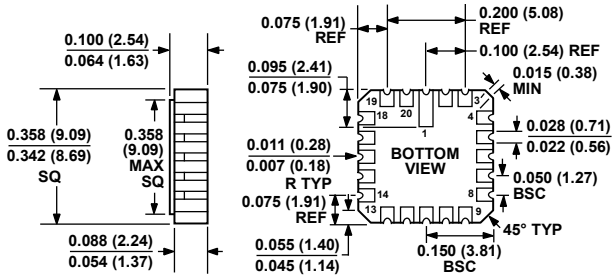
[1] Output offset voltage and output offset voltage drift are given as RTI figures.

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

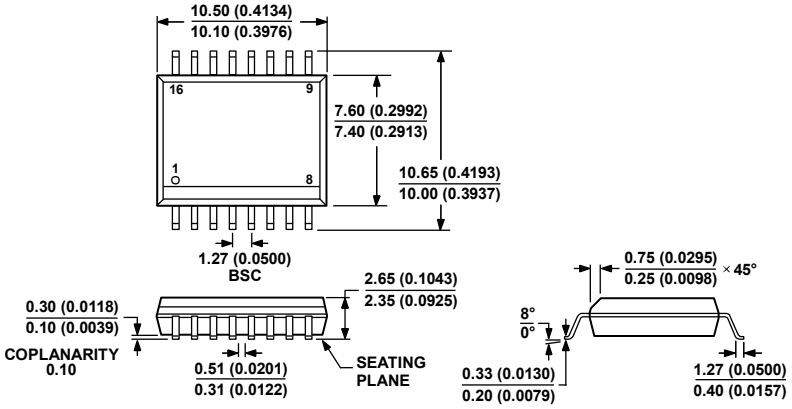
Figure 55. 16-Lead Side-Brazed Ceramic Dual In-Line [SBDIP]
(D-16)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

022106-A

Figure 56. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 57. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD524AD	−40°C to +85°C	16-Lead SBDIP	D-16
AD524ADZ[1]	−40°C to +85°C	16-Lead SBDIP	D-16
AD524AE	−40°C to +85°C	20-Terminal LCC	E-20
AD524AR-16	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD524AR-16-REEL	−40°C to +85°C	16-Lead SOIC_W, 13" Tape and Reel	RW-16
AD524AR-16-REEL7	−40°C to +85°C	16-Lead SOIC_W, 7" Tape and Reel	RW-16
AD524ARZ-16[1]	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD524ARZ-16-REEL7[1]	−40°C to +85°C	16-Lead SOIC_W, 7″Tape and Reel	RW-16
AD524BD	−40°C to +85°C	16-Lead SBDIP	D-16
AD524BDZ[1]	−40°C to +85°C	16-Lead SBDIP	D-16
AD524BE	−40°C to +85°C	20-Terminal LCC	E-20
AD524CD	−40°C to +85°C	16-Lead SBDIP	D-16
AD524CDZ[1]	−40°C to +85°C	16-Lead SBDIP	D-16
AD524SD	−55°C to +125°C	16-Lead SBDIP	D-16
AD524SD/883B	−55°C to +125°C	16-Lead SBDIP	D-16
5962-8853901EA[2]	−55°C to +125°C	16-Lead SBDIP	D-16
AD524SE/883B	−55°C to +125°C	20-Terminal LCC	E-20
AD524SCHIPS	−55°C to +125°C	Die	

[1] Z = RoHS Compliant Part.
[2] Refer to the official DESC drawing for tested specifications.